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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,883	03/28/2001	Finbarr Denis Long	SRT-022	1043

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EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,883	LONG ET AL.	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-15 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-26* is/are allowed.

6)☒ Claim(s) *1,3,4,7,8,10-14 and 19* is/are rejected.

7)☒ Claim(s) *2,9,and15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4, 7, 8, 10-14, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Collins et al., U.S. Patent 5,963,745, hereinafter referred to as "Collins".

3. Referring to claim 1, Collins teaches a parallel array processor that provides the capability to reconfigure in the event of a faulty processing element or node, this is interpreted as a fault-tolerant data processing apparatus (See Col. 2, lines 53-59 and Col. 15, lines 28-29). Collins teaches a parallel array processor with a plurality of chips each with a plurality of PME microcomputers that can operate in SIMD mode which has each processor are commanded from a single instruction stream, this is interpreted as a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously (See Col. 7, lines 25-30 and lines 50-55, Col. 11, lines 51-56, and Col. 12, lines 7-25). Collins teaches each chip of PMEs being considered a node which includes I/O. Each of the nodes is connected via a modified hypercube to each other and one type of I/O class consists of data that must broadcast

to each other, this is as interpreted as an I/O node in communication with at least one of the plurality of data processing elements (See Col. 12, lines 18-20, Col. 14, lines 19-22, and Col. 15, lines 15-22). Collins also teaches a fully distributed I/O programmable router for routing I/O in the modified hypercube setup where I/O communications are asynchronous, this is interpreted as a switching fabric communicating transactions asynchronously between at least one of the plurality of data processing elements and the I/O node (See Col. 14, lines 16-26 and lines 65-67, and Col. 36, lines 40-41).

4. Referring to claim 3, Collins teaches each chip comprising microcomputers, this is interpreted as wherein each of the plurality of data processing elements comprises a central processing unit (See Col. 12, lines 13-14).

5. Referring to claim 4, Collins discloses each chip comprising a plurality of PMEs, this is interpreted as wherein the CPU further comprises a plurality of processors (See Col. 7, lines 25-30, and Col. 12, lines 13-14).

6. Referring to claim 7, Collins teaches each chip having a broadcast and control interface with internal and external communication paths, this is interpreted as wherein a channel adapter interconnects the I/O node to the switching fabric (See Col. 12, lines 15-18).

7. Referring to claim 8, Collins discloses each chip having its own broadcast and control interface with internal and external communications paths and each having the fully distributed I/O programmable router, this interpreted as wherein a plurality of channel adapters interconnect, respectively, each of the plurality of data processing elements to the switching fabric (See Col. 12, lines 15-18 and Col. 14, lines 65-67).

8. Referring to claim 10, Collins teaches each PME's data is input to and output from the main store under Direct Memory Access control, this is interpreted as further comprising a plurality of direct memory access engines in communication with the switching fabric (See Col. 27, lines 19-23).

9. Referring to claim 11, Collins discloses PME send messages by addressing a PME, this is interpreted as wherein the plurality of data processing elements are identified by a node address (See Col. 14, lines 27-37).

10. Referring to claim 12, Collins discloses that any PME can send information through the network to any other PME with addresses, this is interpreted as wherein each the plurality of data processing elements is individually identified by a respective device address (See Col. 42, lines 40-51).

11. Referring to claims 13, Collins discloses packets are used for routing I/O data, this is interpreted as wherein the transaction comprises at least one information packet (See Col. 42, lines 40-51).

12. Referring to claim 14, Collins teaches a method for a parallel array processor that provides the capability to reconfigure in the event of a faulty processing element or node, this is interpreted as a method for a fault-tolerant digital data processing (See Col. 2, lines 53-59 and Col. 15, lines 28-29). Collins teaches a parallel array processor with a plurality of chips each with a plurality of PME microcomputers that can operate in SIMD mode which has each processor are commanded from a single instruction stream (See Col. 7, lines 25-30 and lines 50-55, Col. 11, lines 51-56, and Col. 12, lines 7-25). Collins teaches each chip of PMEs being considered a node which includes I/O. Each of the nodes is connected via a modified hypercube to each other and one type of I/O class consists of data that must broadcast to each other, this is as interpreted generating, by plurality of data processing elements, identical transactions each having an I/O node address (See Col. 12, lines 18-20, Col. 14, lines 19-22, and Col. 15, lines 15-22). Collins also teaches a fully distributed I/O programmable router for routing I/O in the modified hypercube setup where I/O communications are asynchronous, this is interpreted as a communicating the identical transactions asynchronously on a switching fabric to the I/O node-identified by the I/O node-address (See Col. 14, lines 16-26 and lines 65-67, and Col. 36, lines 40-41).

13. Referring to claim 19, Collins discloses each chip having its own broadcast and control interface with internal and external communications paths and each having the fully distributed I/O programmable router, this interpreted as communicating each of the identical transactions from each of the plurality of data processing elements to each of a plurality of channel adapters, communicating each of the identical transactions from each of the plurality of channel adapters to the switching fabric, communicating the identical transaction from the switching fabric to a channel adapter, and communicating the identical transaction from the channel adapter to the I/O node (See Col. 12, lines 15-18 and Col. 14, lines 65-67).

Allowable Subject Matter

14. Claims 20-26 are allowed.

15. Claims 2, 9, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments, see pages 2-6 of response, filed 24 June 2005, with respect to the rejection(s) of claim(s) 1-4, 7-15, and 19-26 under 35 U.S.C. 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of new found prior art, see above rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
September 13, 2005

ROBERT BEAUSOLIEL
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